



## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s)	:	Raaijmakers et al.	)
Appl. No.	:	09/887,199	)
Filed	:	June 21, 2001	)
For	:	METHOD OF FABRICATING	)
		TRENCH ISOLATION	)
		STRUCTURES FOR	)
		INTEGRATED CIRCUITS	)
		USING ATOMIC LAYER	)
		DEPOSITION	)
Group Art Unit:		2814	)
Class/Sub-Class:		438/435000	)
Examiner :		Anh D. Mai	_

# COMMENTS ON EXAMINER'S STATEMENT OF REASONS FOR ALLOWANCE

Assistant Commissioner for Patents Washington, D.C. 20231

## Dear Sir:

Applicants note that the title of the patent application listed on Form PTOL-85 is incorrect. The title, as amended in the Response to Office Action filed on November 5, 2003, should read METHOD OF FABRICATING TRENCH ISOLATION STRUCTURES FOR INTEGRATED CIRCUITS USING ATOMIC LAYER DEPOSITION.

In addition, Applicants respectfully disagree with the Examiner's Statement of Reasons for Allowance to the extent that there is any implication that the patentability of the claims rests on the recitation of a single feature. Rather, it is the recited combination of features that makes the claims patentable. For instance, Claim 13 recites a method of fabricating trench isolation structures between integrated electrical devices in a semiconductor substrate, comprising:

placing a semiconductor substrate in a reaction chamber, the semiconductor substrate comprising trenches; and

completely filling the trenches with insulating material by atomic layer deposition to form a trench isolation structure, the atomic layer deposition process comprising a plurality of primary cycles, each primary cycle comprising, in sequence:

Appl. No.

ASMMC.005AUS

Filed

June 21, 2001

:

introducing a first vapor-phase reactant to the substrate, thereby forming no more than about one monolayer of a first reactant species conforming at least to surfaces of the trenches;

removing excess first vapor-phase reactant and byproduct from the reaction chamber;

introducing a second vapor-phase reactant to the substrate, thereby reacting with the first reactant species conforming at least to the surfaces of the trenches; and

removing excess second vapor-phase reactant and byproduct from the reaction chamber,

wherein filling the trenches further comprises a plurality of secondary cycles, each secondary cycle comprising, in sequence:

introducing a third vapor-phase reactant to the substrate, thereby forming no more than about one monolayer of a third reactant species conforming at least to surfaces of the trenches, the third reactant species being different from the first reactant species;

removing excess third vapor-phase reactant and byproduct from the reaction chamber;

introducing a fourth vapor-phase reactant to the substrate, thereby reacting with the third reactant species conforming at least to the surfaces of the trenches; and

removing excess fourth vapor-phase reactant and byproduct from the reaction chamber,

wherein the primary cycles deposit silicon oxide and the secondary cycles deposit aluminum oxide and filling the trench comprises depositing aluminum oxide to form the insulating material comprising silicon oxide and between about 26% and 34% aluminum oxide by weight.

Accordingly, Applicants submit that Claim 13 is allowable because the prior art does not teach or suggest the combination of features as recited by this claim. Likewise, the other claims of

Appl. No. : ASMMC.005AUS Filed : June 21, 2001

the present application are also allowable because they each recite a combination of features that are not taught or suggested by the prior art.

By:

Respectfully submitted,

KNOBBE, MARTENS, OLSON & BEAR, LLP

Dated: September 22, 2004

Andrew N. Merickel Registration No. 53,317 Attorney of Record Customer No. 20,995

(415) 954-4114

W:\DOC\$\ANM\ANM-7409.DOC 092204



Case Docket No. ASMMC.005AUS

Date: September 22, 2004

#### IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s)

Raaijmakers et al.

Appl. No.

09/887,199

Filed

June 21, 2001

For

METHOD OF FABRICATING

TRENCH ISOLATION STRUCTURES FOR

INTEGRATED CIRCUITS USING ATOMIC LAYER

**DEPOSITION** 

Group Art Unit

2814

Class/Sub-Class:

438/435000

Examiner

Anh D. Mai

I hereby certify that this correspondence and all marked attachments are being deposited with the United States Postal Service as first class mail in an envelope addressed to: Mail Stop Issue Fee, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on

September 22, 2004

(Date)

Andrew N. Merickel, Reg. No. 53,317

### TRANSMITTAL LETTER

MAIL STOP ISSUE FEE **Commissioner for Patents** P.O. Box 1450 Alexandria, VA 22313-1450

Dear Sir:

Enclosed for filing is the Issue Fee for the above-identified application:

- Form PTOL-85, adjusted to include the correct title, as amended in the Amendment and (X) Response to Office Action filed by Applicants on November 5, 2003.
- Comments on Examiner's Statement of Reasons for Allowance. (X)
- (X) A check in the amount of \$1,660 to cover the issue fee, publication fee, and advanced order of copies is enclosed.
- (X) The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment, to Account No. 11-1410.

Case Docket No. ASMMC.005AUS Date: September 22, 2004

(X) Return prepaid postcard.

Andrew N. Merickel Registration No. 53,317 Attorney of Record Customer No. 20,995 (415) 954-4114

W:\DOC\$\ANM\ANM-7407.DOC 092204